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3-phase Inverter Power Module for the Compact IPM Series

AND9390/D

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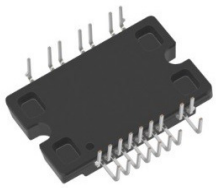
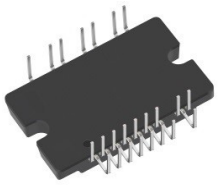
APPLICATION NOTE



DIP−S



DIP−S6

Introduction

This application note provides practical guidelines for designing with the Compact IPM series power modules.

This series of Intelligent Power Modules (IPM) for 3−phase motor drives contains a three−phase inverter stage, gate drivers and a thermistor.

Key Functions

- Highly integrated power module containing an inverter power stage for a high voltage 3−phase inverter in a small dual in−line (DIP) package.
- Output stage uses IGBT/FRD technology and implements Under Voltage Protection (UVP) and Over−current Protection (OCP) with a fault detection output flag. Internal bootstrap diodes are provided for the high−side drivers.
- Separate pins for each of the three low−side emitter terminals.
- Thermistor for substrate temperature measurement.
- All control inputs and status outputs have voltage levels compatible with microcontrollers.
- Single V_{DD} power supply due to internal bootstrap circuit for high−side gate driver circuit.
- Mounting holes for easy assembly of heat sink with screws.

A simplified block diagram of a motor control system is shown in Figure 1.

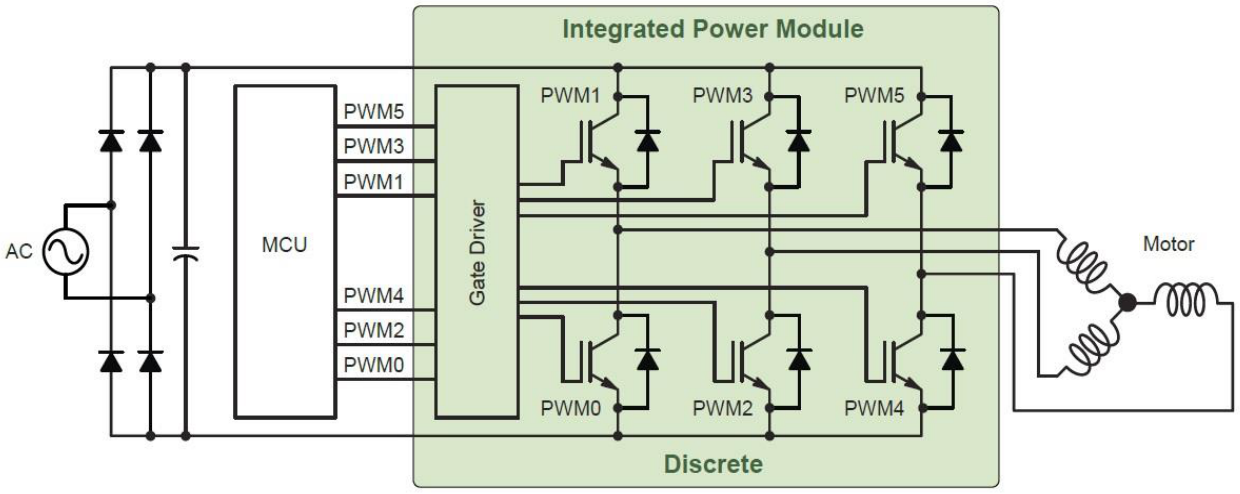


Figure 1. Motor Control System Block Diagram

PRODUCT DESCRIPTION

Table 1 gives an overview of the available devices in the Compact IPM series. For package drawing, please refer to Package Outline chapter.

Table 1. DEVICE OVERVIEW

Device	STK5C4U332J−E	NFAQ0560R43T	NFAQ0860L36T	NFAQ1060L33T NFAQ1060L36T	NFAQ1560R43T(L)
Feature	triple shunts				
Package	DIP−S	DIP−S6 (Standard with stopper)	DIP−S6 (Short)	DIP−S6 (Standard/short)	DIP−S6 (Standard with stopper)
Voltage (VCEmax.)	600 V				
Current (Ic)	3 A	5 A	8 A	10 A	15 A
Peak current (Ic)	6 A	10 A	16 A	20 A	30 A
Isolation voltage	2000 V				
Shunt resistance	External				

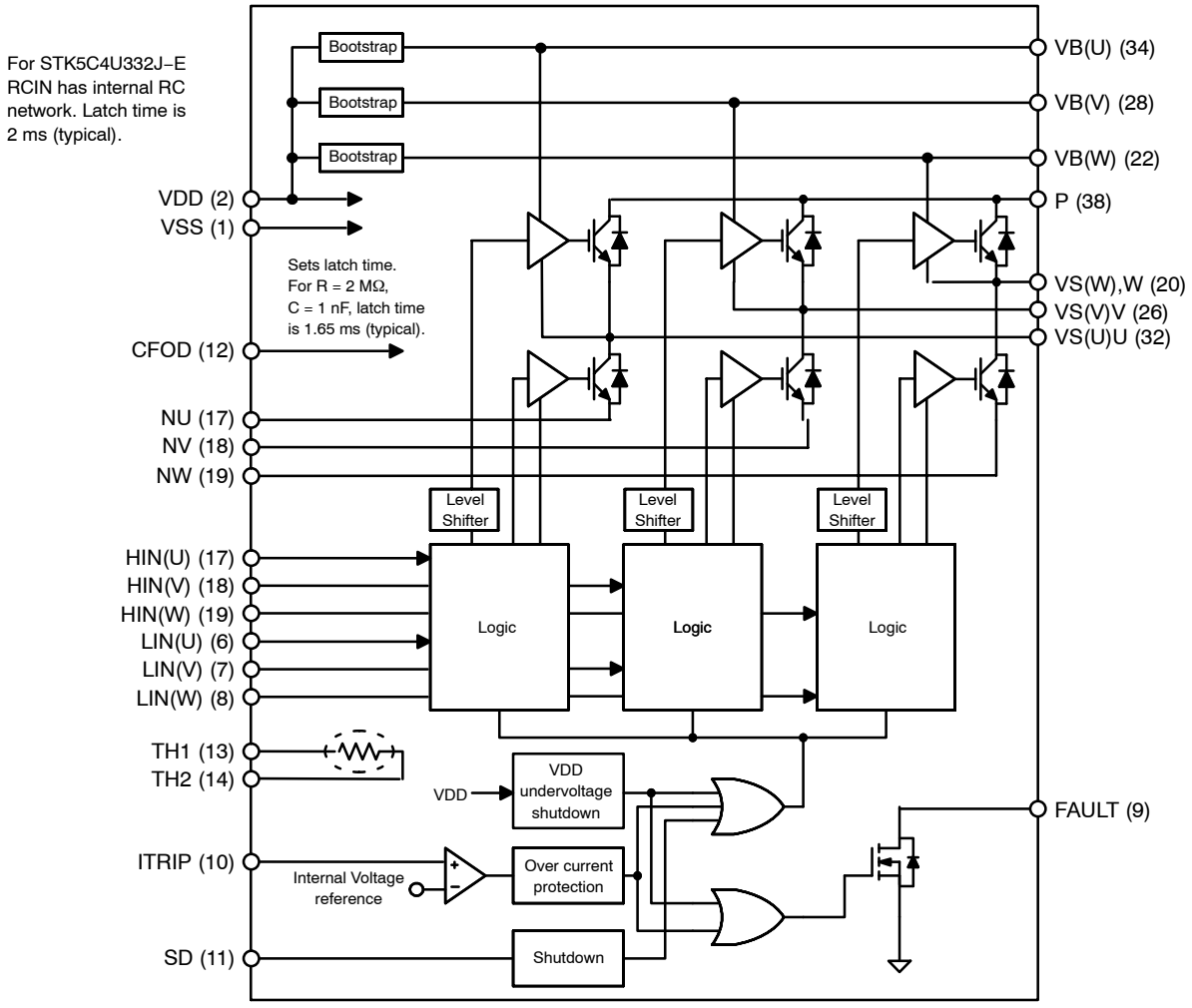


Figure 2. Compact IPM Series Internal Diagram

Three bootstrap circuits generate the voltage needed for driving the high−side IGBTs. The boost diodes are internal to the part and sourced from VDD (15 V). There is an internal level shift circuit for the high−side drive signals allowing all control signals to be driven directly from GND levels common with the control circuit such as the microcontroller without requiring external isolation with photocouplers.

PERFORMANCE TEST GUIDELINES

The methods used to test some datasheet parameters are shown in Figures 3 to 7.

Switching Time Definition and Performance Test Method

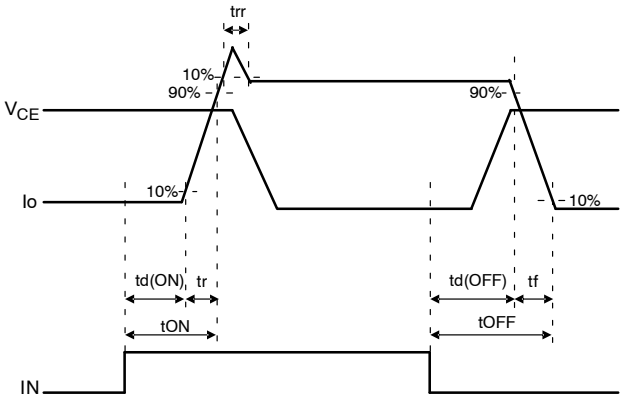


Figure 3. Switching Time Definition

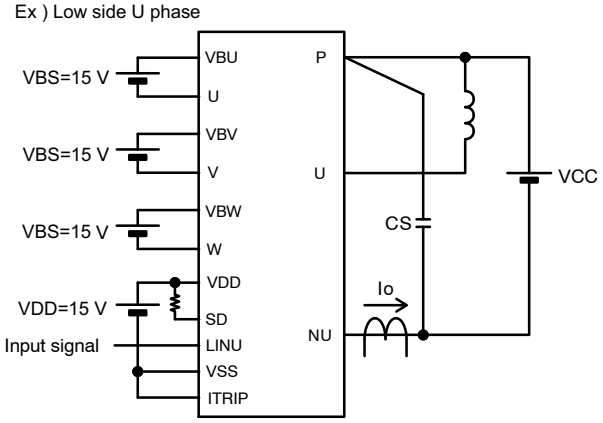


Figure 4. Evaluation Circuit (Inductive Load)

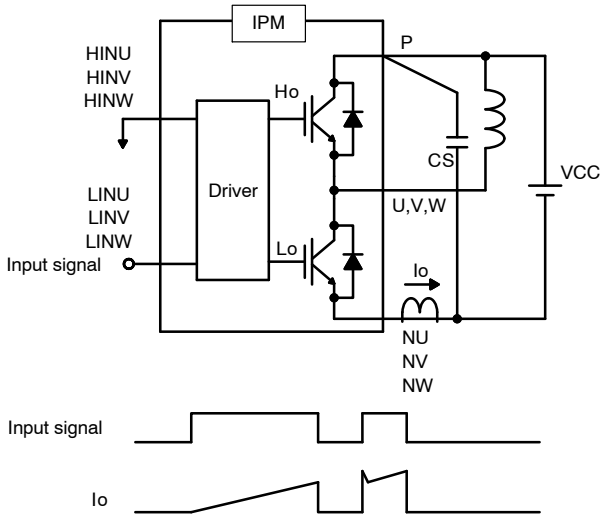


Figure 5. Switching Loss Measurement Circuit

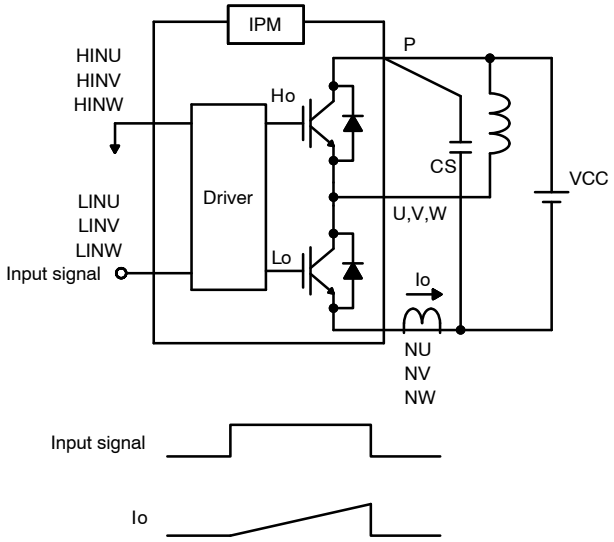


Figure 6. Reverse Bias Safe Operating Area Measurement Circuit

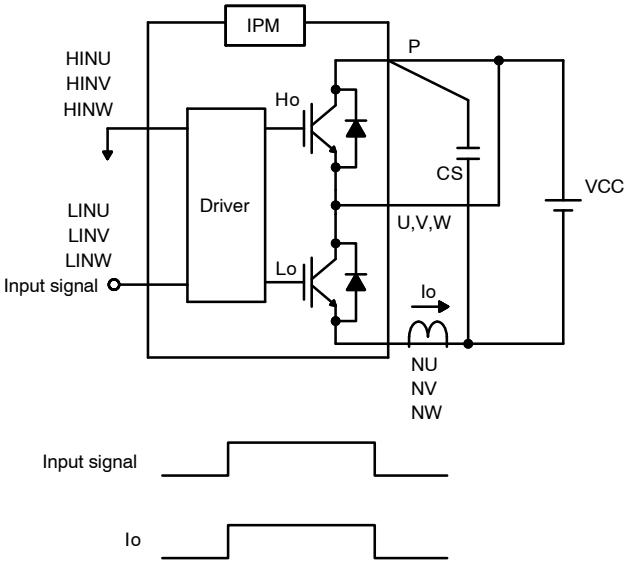


Figure 7. Short Circuit Operating Area Measurement Circuit

Thermistor Characteristics

The TH1 and TH2 pins are connected to a thermistor mounted on the module substrate. The thermistor is used to sense the internal substrate temperature. It has the following characteristics.

Table 2. NTC THRMISTOR SPECIFICATION

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resistance	R_{25}	T_C = 25°C	99	100	101	kΩ
Resistance	R_{100}	T_C = 100°C	5.18	5.41	5.60	kΩ
Temperature Range			−40		+125	°C

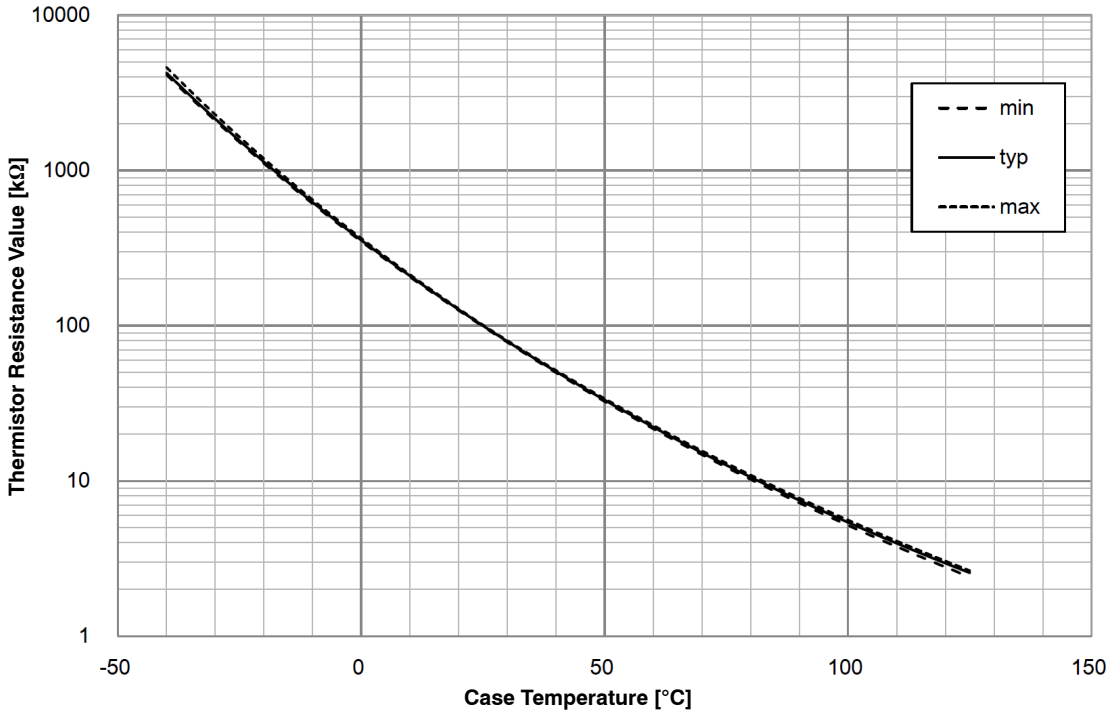


Figure 8. NTC Thermistor Resistance versus Temperature

Table 3. NTC THERMISTOR RESISTANCE VALUES

Tc [°C]	Resistance Value [kΩ]			Tc [°C]	Resistance Value [kΩ]			Tc [°C]	Resistance Value [kΩ]		
	Min	Typ	Max		Min	Typ	Max		Min	Typ	Max
−40	4130.00	4251.00	4612.34	16	152.51	154.60	156.96	72	13.69	14.10	14.52
−39	3851.00	3962.00	4290.13	17	145.20	147.20	149.28	73	13.19	13.60	14.00
−38	3593.00	3695.00	3992.58	18	138.27	140.10	142.02	74	12.71	13.11	13.51
−37	3353.00	3447.00	3717.65	19	131.72	133.40	135.16	75	12.25	12.64	13.03
−36	3131.00	3218.00	3463.47	20	125.51	127.00	128.66	76	11.81	12.19	12.57
−35	2925.00	3005.00	3228.35	21	119.63	121.00	122.51	77	11.39	11.76	12.13
−34	2733.00	2807.00	3010.74	22	114.05	115.40	116.69	78	10.99	11.35	11.71
−33	2556.00	2624.00	2809.21	23	108.77	110.00	111.17	79	10.60	10.96	11.30
−32	2391.00	2454.00	2622.49	24	103.75	104.80	105.95	80	10.23	10.58	10.91
−31	2238.00	2296.00	2449.39	25	99.00	100.00	101.00	81	9.87	10.21	10.54
−30	2095.00	2149.00	2288.84	26	94.40	95.40	96.40	82	9.53	9.86	10.18
−29	1962.00	2012.00	2139.84	27	90.04	91.04	92.03	83	9.20	9.52	9.83
−28	1839.00	1885.00	2001.49	28	85.90	86.90	87.88	84	8.88	9.20	9.50
−27	1724.00	1767.00	1872.97	29	81.97	82.97	83.94	85	8.57	8.89	9.18
−26	1617.00	1656.00	1753.51	30	78.25	79.23	80.20	86	8.28	8.59	8.87
−25	1517.00	1554.00	1642.43	31	74.71	75.69	76.65	87	8.00	8.30	8.58
−24	1424.00	1458.00	1538.88	32	71.35	72.32	73.27	88	7.73	8.02	8.29
−23	1338.00	1369.00	1442.51	33	68.16	69.12	70.05	89	7.47	7.76	8.02
−22	1257.00	1286.00	1352.78	34	65.13	66.07	67.00	90	7.22	7.50	7.75
−21	1181.00	1208.00	1269.20	35	62.25	63.18	64.09	91	6.98	7.25	7.50
−20	1110.00	1135.00	1191.30	36	59.51	60.42	61.33	92	6.75	7.02	7.26
−19	1044.00	1068.00	1118.67	37	56.91	57.81	58.70	93	6.52	6.79	7.02
−18	982.70	1004.00	1050.92	38	54.43	55.31	56.19	94	6.31	6.57	6.80
−17	925.10	945.00	987.69	39	52.07	52.94	53.80	95	6.10	6.36	6.58
−16	871.10	889.60	928.65	40	49.83	50.68	51.53	96	5.90	6.15	6.37
−15	820.40	837.80	873.51	41	47.70	48.53	49.37	97	5.71	5.96	6.17
−14	772.93	789.30	821.97	42	45.67	46.49	47.31	98	5.53	5.77	5.97
−13	728.49	743.90	773.79	43	43.73	44.53	45.34	99	5.35	5.59	5.78
−12	686.88	701.30	728.72	44	41.89	42.67	43.47	100	5.18	5.41	5.60
−11	647.89	661.50	686.55	45	40.13	40.90	41.68	101	5.01	5.24	5.42
−10	611.35	624.10	647.07	46	38.46	39.21	39.98	102	4.85	5.08	5.26
−9	577.04	589.00	610.04	47	36.86	37.60	38.35	103	4.70	4.92	5.09
−8	544.86	556.20	575.36	48	35.34	36.06	36.80	104	4.55	4.77	4.94
−7	514.67	525.30	542.85	49	33.89	34.60	35.31	105	4.41	4.62	4.79
−6	486.34	496.30	512.38	50	32.50	33.19	33.90	106	4.27	4.48	4.64
−5	459.73	469.10	483.79	51	31.18	31.86	32.55	107	4.14	4.35	4.50
−4	434.77	443.50	457.01	52	29.92	30.58	31.26	108	4.01	4.22	4.36
−3	411.31	419.50	431.86	53	28.72	29.36	30.03	109	3.89	4.09	4.23
−2	389.25	396.90	408.25	54	27.57	28.20	28.85	110	3.77	3.97	4.10
−1	368.50	375.60	386.06	55	26.47	27.09	27.72	111	3.66	3.85	3.98
0	348.97	355.60	365.20	56	25.42	26.03	26.64	112	3.55	3.73	3.86
1	330.58	336.80	345.57	57	24.42	25.01	25.62	113	3.44	3.62	3.75
2	313.25	319.10	327.11	58	23.46	24.04	24.63	114	3.33	3.52	3.64
3	296.94	302.40	309.74	59	22.55	23.11	23.69	115	3.24	3.42	3.53
4	281.57	286.70	293.39	60	21.67	22.22	22.79	116	3.14	3.32	3.43
5	267.08	271.80	278.00	61	20.84	21.37	21.92	117	3.05	3.22	3.33
6	253.42	257.80	263.50	62	20.04	20.56	21.10	118	2.96	3.13	3.23
7	240.54	244.70	249.84	63	19.27	19.78	20.31	119	2.87	3.04	3.14
8	228.39	232.20	236.97	64	18.54	19.04	19.55	120	2.79	2.95	3.05
9	216.91	220.50	224.83	65	17.83	18.32	18.82	121	2.71	2.87	2.96
10	206.08	209.40	213.38	66	17.16	17.64	18.13	122	2.63	2.79	2.88
11	195.85	198.90	202.58	67	16.52	16.99	17.46	123	2.55	2.71	2.80
12	186.18	189.00	192.38	68	15.91	16.36	16.83	124	2.48	2.63	2.72
13	177.05	179.70	182.76	69	15.32	15.76	16.21	125	2.41	2.56	2.64
14	168.41	170.90	173.67	70	14.75	15.18	15.63				
15	160.24	162.50	165.08	71	14.21	14.63	15.06				

PROTECTION FUNCTIONS

This chapter describes the protection functions.

- Over−current protection
- Short circuit protection
- Under voltage lockout (UVLO) protection
- Cross conduction prevention

Over−Current Protection

Compact IPM series modules use an external shunt resistor for the OCP functionality. As shown in Figure 9, the emitters of all three low−side IGBTs are brought out to module pins. The external OCP circuit consists of a shunt resistor and a RC filter network. If the application uses three separate shunts, an op−amp circuit is used to monitor the three separate shunts and provide an over−current signal.

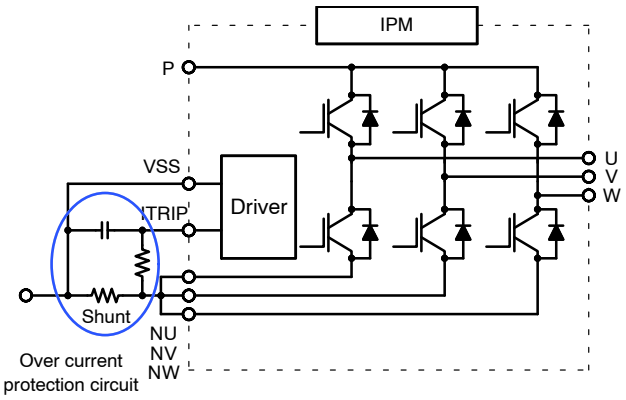


Figure 9. Over−Current Protection Circuit

The OCP function is implemented by comparing the ITRIP input voltage with an internal reference voltage of 0.49 V (typ). If the voltage on this terminal exceeds the trip level, an OCP fault is triggered. This voltage is the same as the voltage across the shunt resistor.

NOTE: The current value of the OCP needs to be set by correctly sizing the external shunt resistor to less than the module's maximum current rating.

When an OCP fault is detected, all internal gate drive signals for the IGBTs become inactive and the fault signal output is activated. The FAULT signal has an open drain output, so when there is a fault, the output is pulled low.

A RC filter is used on the ITRIP input to prevent an erroneous OCP detection due to normal switching noise or recovery diode current. The time constant of that RC filter should be set to a value between 1.5 μs to 2 μs. In any case the time constant must be shorter than the IGBTs short current safe operating area (SCSOA). Please refer to Data Sheet for SCSOA. The resulting OCP level due to the filter time constant is shown in Figure 10.

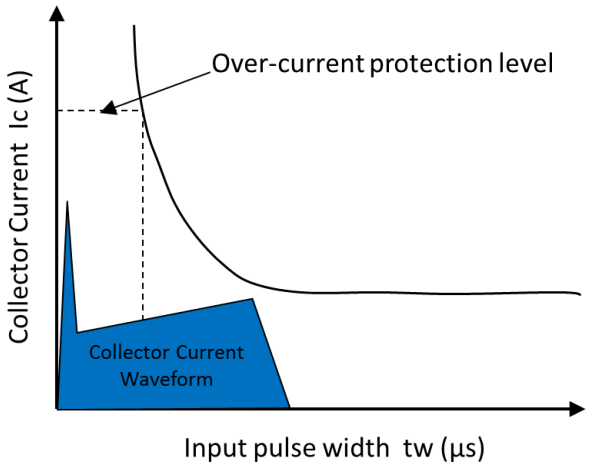


Figure 10. Filter Time Constant

For optimal performance all traces around the shunt resistor need to be kept as short as possible.

Figure 11 shows the sequence of events in case of an OCP event.

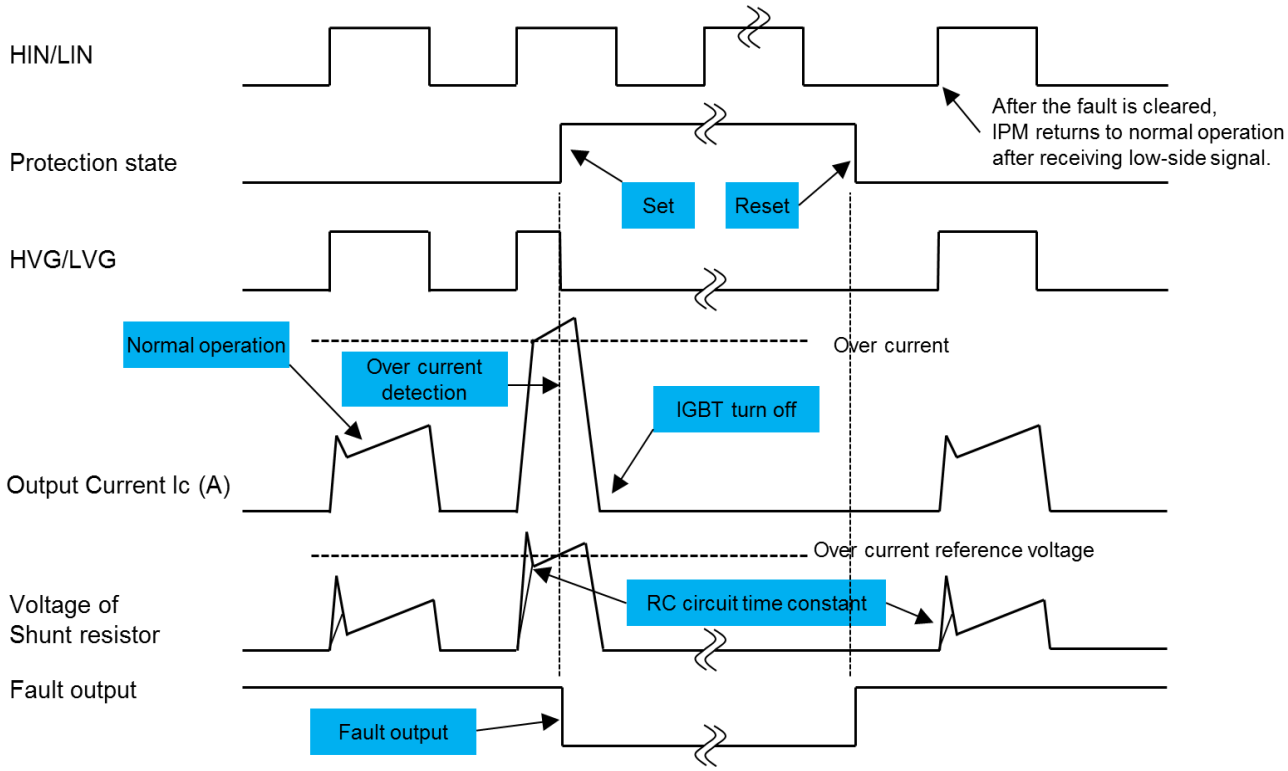


Figure 11. Overcurrent Protection Timing Diagram

Under Voltage Lockout Protection

The UVLO protection is designed to prevent unexpected operating behavior as described in Table 4. Both High−side and Low−side have undervoltage protection. The low−side UVLO condition is indicated on the FAULT output. During the low−side UVLO state the FAULT output is continuously driven low. A high−side UVLO condition is not indicated on the FAULT output.

Table 4. MODULE OPERATION ACCORDING TO VDD VOLTAGE

VDD Voltage (typ. Value)	Operation Behavior
< 13.0 V	As the voltage is lower than the UVLO threshold the control circuit is not fully turned on. A perfect functionality cannot be guaranteed.
13.0 V – 13.5 V	IGBTs can work, however conduction and switching losses increase due to low voltage gate signal.
13.5 V – 16.5 V	Recommended conditions.
16.5 V – 20.0 V	IGBTs can work. Switching speed is faster and saturation current higher, increasing short−circuit broken risk.
> 20.0 V	Control circuit is destroyed. Absolute max. rating is 20 V.

The sequence of events in case of a low−side UVLO event (IGBTs turned off and active fault output) is shown in Figure 12. Figure 13 shows the same for a high−side UVLO (IGBTs turned off but no fault output).

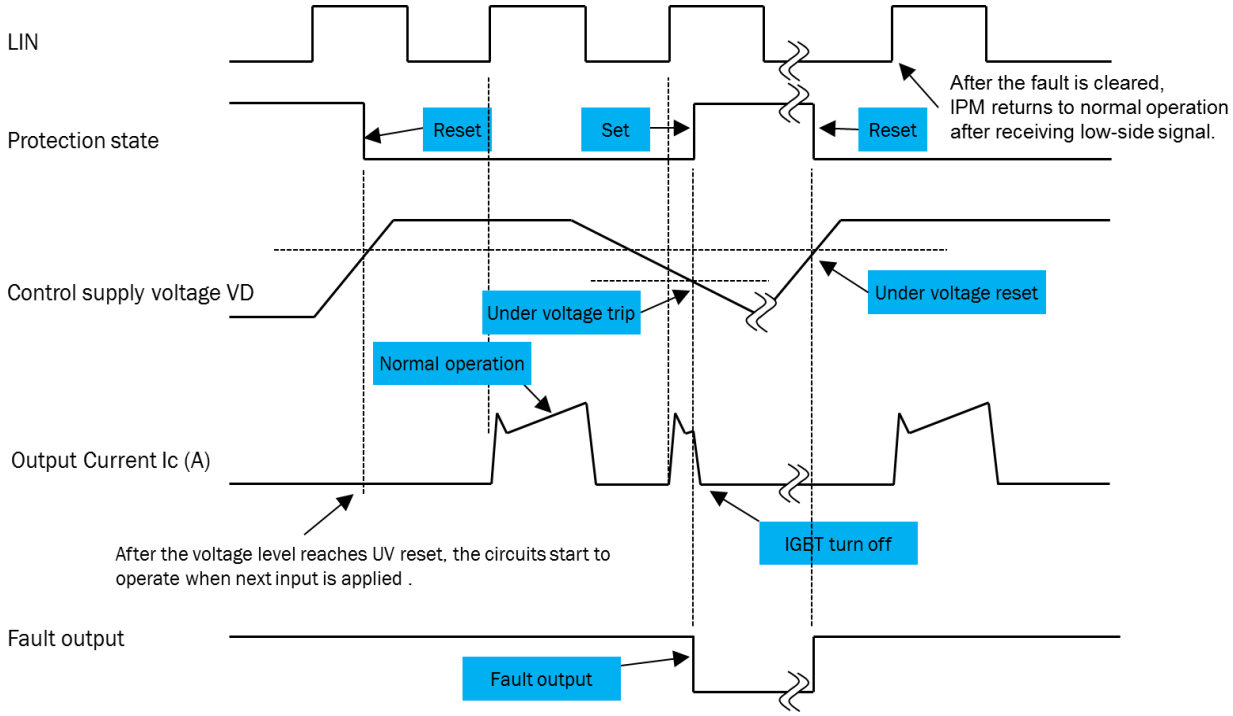


Figure 12. Low−Side UVLO Timing Diagram

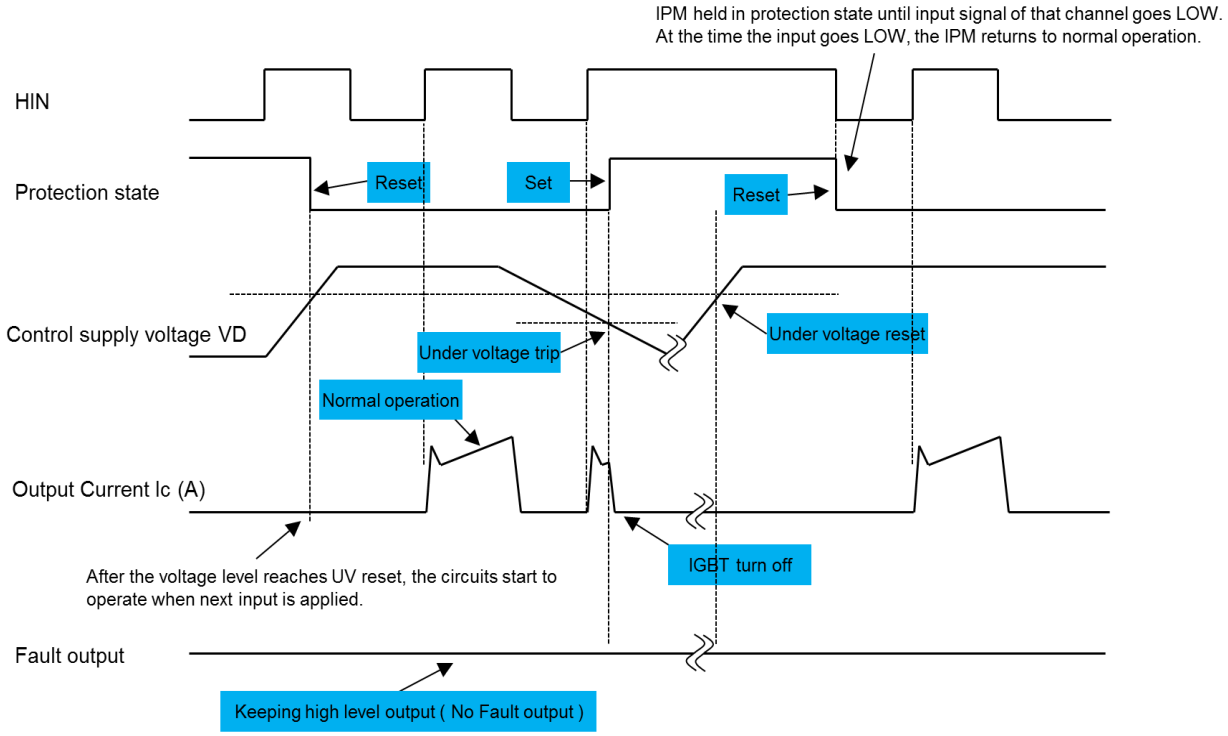


Figure 13. High−Side UVLO Timing Diagram

Cross−Conduction Prevention

The Compact IPM series implements cross−conduction prevention logic at the gate driver to avoid simultaneous drive of the low−side and high−side IGBTs as shown in Figure 14.

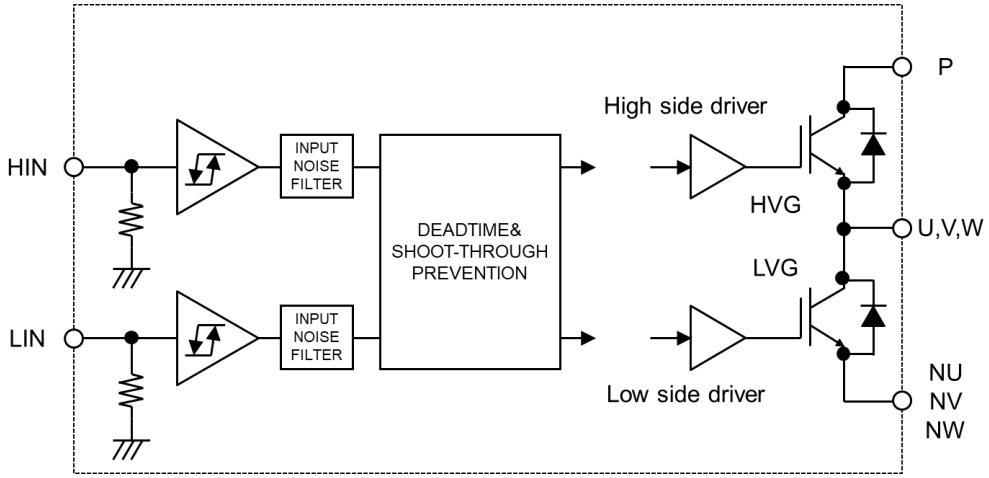


Figure 14. Cross−Conduction Prevention

If both high−side and low−side drive inputs are active (HIGH) the logic prevents both gates from being driven as shown in Figure 15 below.

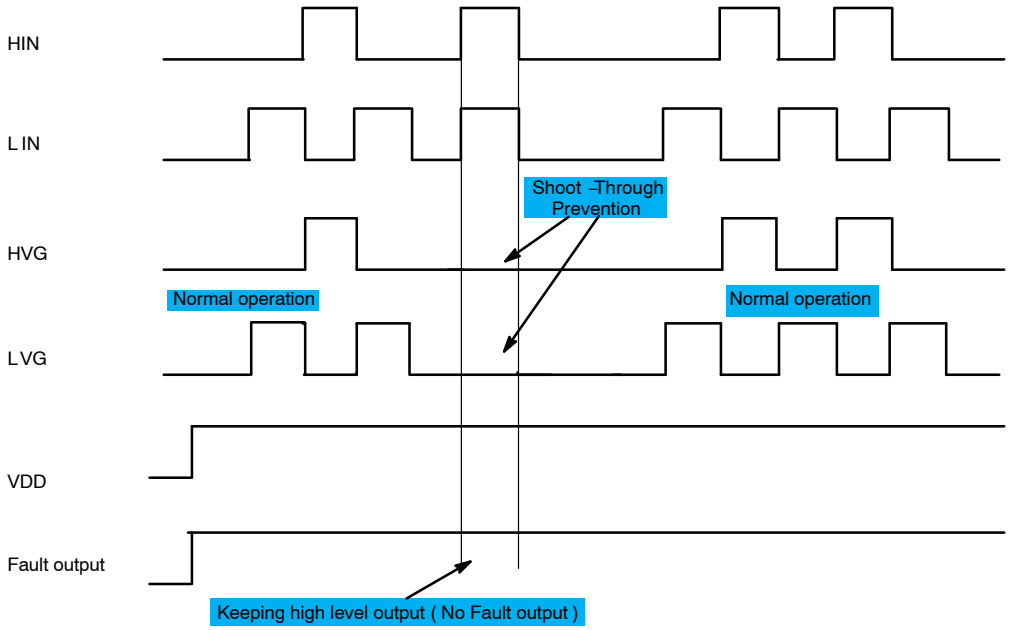


Figure 15. Cross−Conduction Prevention Timing Diagram

Even if cross−conduction on the IGBTs due to incorrect external driving signals is prevented by the circuitry, the driving signals (HIN and LIN) need to include a “dead time”. This period where both inputs are inactive between either one becoming active is required due to the internal delays within the IGBTs.

Figure 16 shows the delay from the HIN−input via the internal high−side gate driver to high−side IGBT, the delay from the LIN−input via the internal low−side gate driver to low−side IGBT and the resulting minimum dead time which is equal to the potential shoot through period:

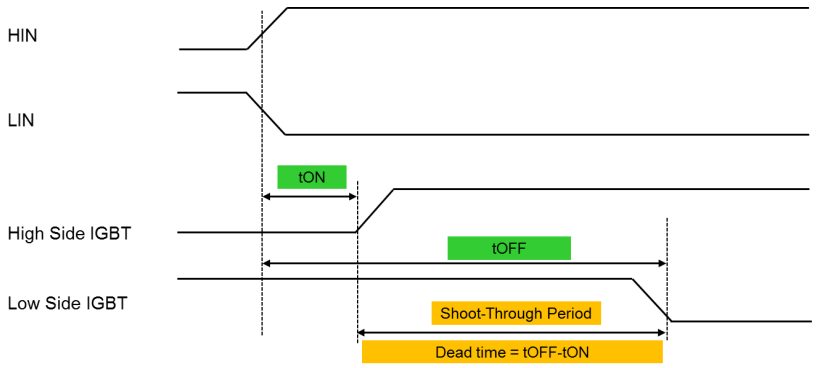


Figure 16. Shoot−Through Period

PCB DESIGN AND MOUNTING GUIDELINES

This chapter provides guidelines for an optimized design and PCB layout as well as module mounting recommendations to appropriately handle and assemble the IPM.

Application (Schematic) Design

Figure 17 gives an overview of the external components and circuits when designing with the Compact IPM series modules.

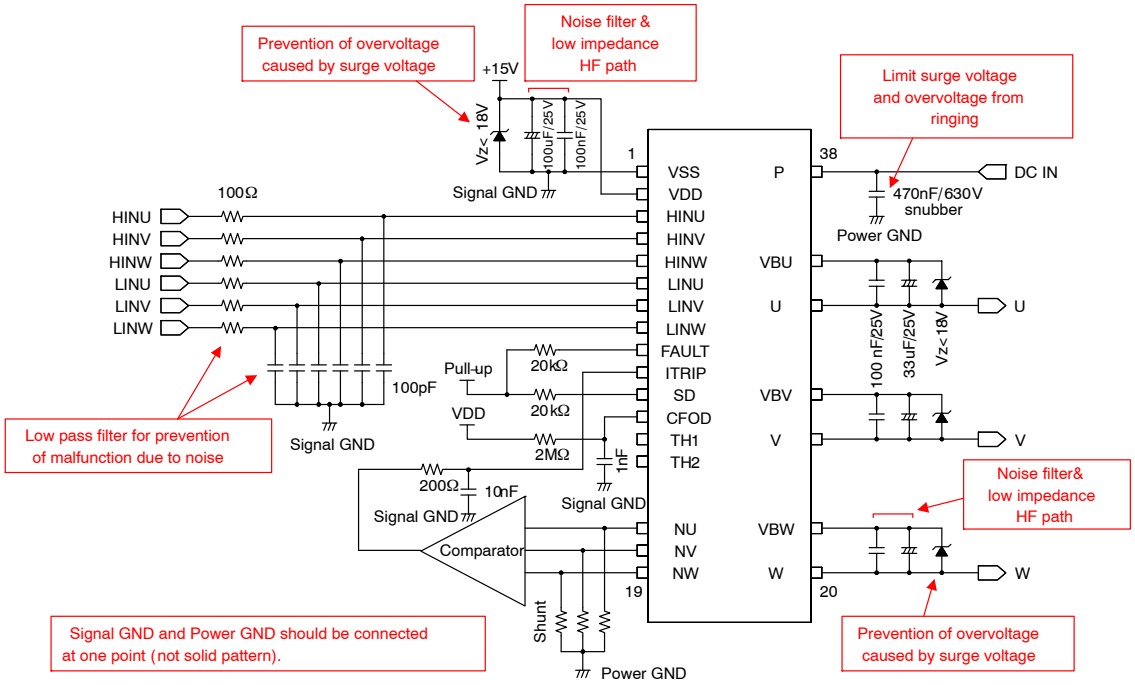


Figure 17. Compact IPM Series Application Circuit

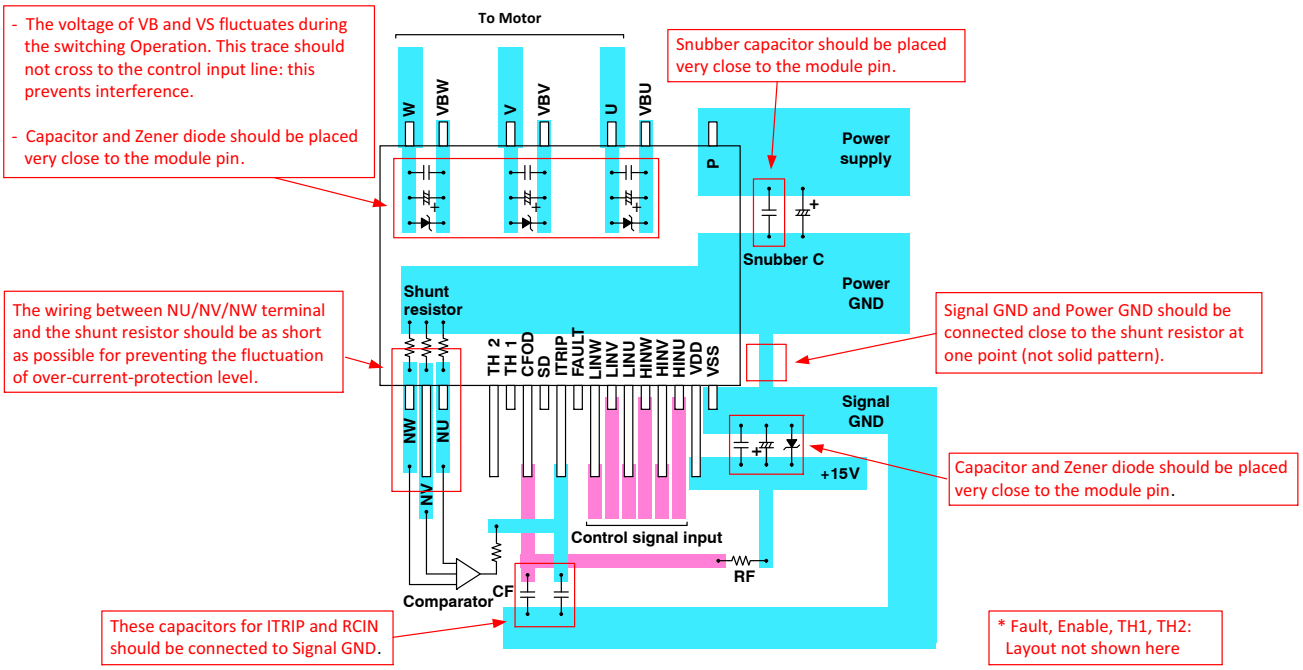


Figure 18. Compact IPM Recommended Layout

Pin by Pin Design and Usage Notes

This section provides pin by pin PCB layout recommendations and usage notes. A complete list of module pins is given in Package Outline chapter.

P NU, NV, NW

DC Power supply terminal for the inverter block. Voltage spikes could be caused by longer traces to these terminals due to the trace inductance, therefore traces are recommended to be as short as possible. In addition a snubber capacitor should be connected as close as possible to the P terminal to stabilize the voltage and absorb voltage surges.

U, V, W

These are the output pins for connecting the 3−phase motor. They share the same GND potential with each of the high−side control power supplies. Therefore they are also used to connect the GND of the bootstrap capacitors. These bootstrap capacitors should be placed as close to the module as possible.

VDD, VSS

These pins provide power to the low−side gate drivers, the protection circuits and the bootstrap circuits. The voltage between these terminals is monitored by the UVLO circuit. The VSS terminal is the reference voltage for the input control signals.

VBU, VBV, VBW

The VBx pins are internally connected to the positive supply of the high−side drivers. The supply needs to be floating and electrically isolated. The boot−strap circuit shown in Figure 19 forms this power supply individually for every phase. Due to integrated boot FET only an external boot capacitor (CB) is required.

CB is charged when the following two conditions are met.

- Low−side signal is input.
- Motor terminal voltage is low level.

The capacitor is discharged while the high−side driver is activated.

Thus CB needs to be selected taking the maximum on time of the high−side and the switching frequency into account.

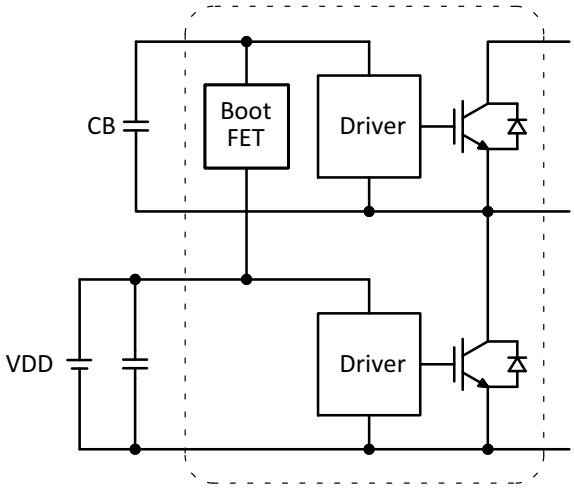


Figure 19. Bootstrap Circuit

The voltages on the high−side drivers are individually monitored by the under voltage protection circuit. If there is a UVLO fault on any given phase, the output on that phase is disabled.

Typically a CB value of less or equal 47uF (±20%) is used. In case the CB value needs to be higher, an external resistor (20 Ω or less) should be used in series with the capacitor to avoid high currents which can cause malfunction of the IPM.

HINU, LINU, HINV, LINV, HINW, LINW

These pins are the control inputs for the power stages. The inputs on HINU/HINV/HINW control the high−side transistors of U/V/W, the inputs on LINU/LINV/LINW control the low−side transistors of U/V/W respectively. The input logic is active HIGH. An external microcontroller can directly drive these inputs without need for isolation.

Simultaneous activation of both low−side and high−side is prevented internally to avoid shoot through at the power stage. However, due to IGBT switching delays the control signals must include a dead−time.

The equivalent input stage circuit is shown in Figure 20.

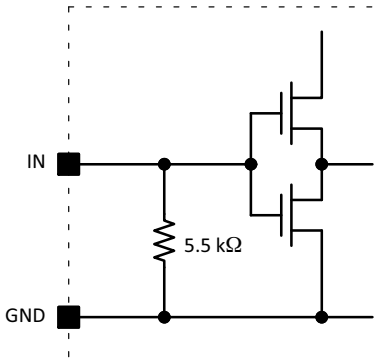


Figure 20. Internal Input Circuit

The output might not respond when the width of the input pulse is less than 1 μs (both ON and OFF).

NOTE: After applying VDD, it is necessary to input the low−side signal for starting the operation.

FAULT

The Fault pin is an active low output (open−drain output). It is used to indicate an internal fault condition of the module. The structure is shown in Figure 21.

The sink current of IoSD during an active fault is nominal 2mA @ 0.1V. Depending on the interface supply voltage, the external pull−up resistor (RP) needs to be selected to set the low voltage below the VIL trip level.

For the commonly used supplies:

- Pull up voltage = 15 V → RP >= 20 kΩ
- Pull up voltage = 5 V → RP >= 6.8 kΩ

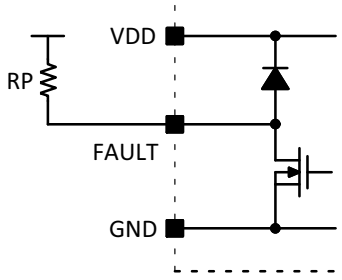


Figure 21. Fault Connection

For a detailed description of the fault operation refer to “PROTECTION FUNCTIONS” chapter.

NOTE: The Fault signal does not permanently latch. After the protection event ended, and the fault clear time (1.65 ms) passed, the module’s operation is re−started by inputting the low−side signal. Therefore the input needs to be driven low externally activated as soon as a fault is detected.

ITRIP

This pin is used to enable an OCP function. When the voltage of this pin exceeds a reference voltage, the OCP function operates. For details of the OCP operation refer to “PROTECTION FUNCTIONS” chapter.

SD

SD pin has shutdown function of the internal gate driver. The gate driver operates when the voltage of this pin is at 2.5 V or more, and stops at 0.8 V or less.

This pin can also be connected to the FAULT pin directly.

TH1, TH2

An internal thermistor to sense the substrate temperature is connected between TH1 and TH2. By connecting an external pull−up resistor to either of TH1 and TH2, and shorting the other and GND, the module temperature can be monitored. Please refer to “Thermistor Characteristics” for details of the thermistor.

NOTE: This is the only means to monitor the substrate temperature indirectly.

CFOD

This pin is used to set the fault clear time.

NFAQxx60xxx Series

By connecting the resistor RF versus VDD and the capacitor CF versus GND, the fault clear time can be set. In condition that RF is 2 MΩ and CF is 1 nF, the fault clear time is 1.65 ms.

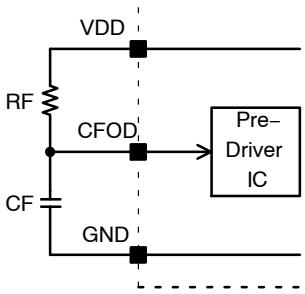


Figure 22. CFOD Circuit (NFAQxx60xxx Series)

To shorten the fault clear time, reduce the value of RF or CF.

STK5C4U332J−E

The resistor and the capacitor for setting the fault clear time are built−in as shown in Figure 23. It is recommended to leave this pin open. In that case, the default fault clear time is 2 ms.

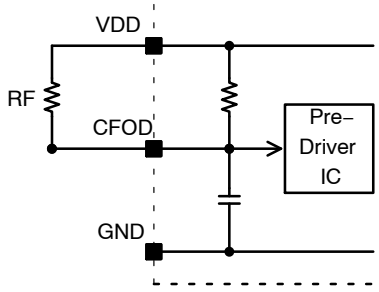


Figure 23. CFOD Circuit (STK5C4U332J−E)

To shorten the fault clear time, connect an external resistor RF between VDD and CFOD.

Heat Sink Mounting and Torque

If a heat sink is used, insufficiently secure or inappropriate mounting can lead to a failure of the heat sink to dissipate heat adequately.

The following general points should be observed when mounting IPM on a heat sink:

1. Verify the following points related to the heat sink:
   - There must be no burrs on aluminum or copper heat sinks.
   - Screw holes must be countersunk.
   - There must be no unevenness in the heat sink surface that contacts IPM.
   - There must be no contamination on the heat sink surface that contacts IPM.
2. Highly thermal conductive silicone grease needs to be applied to the whole back (substrate side) uniformly, and mount IPM on a heat sink. If the device is removed, grease must be applied again.
3. For a good contact between the IPM and the heat sink, the mounting screws should be tightened gradually and sequentially while a left/right balance in pressure is maintained. Either a bind head screw or a truss head screw is recommended. Please do not use tapping screw. We recommend using a flat washer in order to prevent slack.

The standard heat sink mounting condition of the Compact IPM series is as follows.

Table 5. HEAT SINK MOUNTING

Item	Recommended Condition
Pitch	26.0 ± 0.1 mm (refer to Package Outline Diagram)
Screw	Diameter: M3 Screw head types: pan head, truss head, binding head
Washer	Plane washer dimensions: D = 7 mm, d = 3.2 mm and t = 0.5 mm JIS B 1256
Heat sink	Material: Aluminum or Copper Warpage (the surface that contacts IPM): −50 to 50 μm Screw holes must be countersunk. No contamination on the heat sink surface that contacts IPM.

Table 5. HEAT SINK MOUNTING (continued)

Item	Recommended Condition
Torque	Temporary tightening : 50 to 60 % of final tightening on first screw Temporary tightening : 50 to 60 % of final tightening on second screw Final tightening : 0.4 to 0.6 Nm on first screw Final tightening : 0.4 to 0.6 Nm on second screw
Grease	Silicone grease. Thickness : 50 to 100 μm Uniformly apply silicon grease to whole back. Thermal foils are only recommended after careful evaluation. Thickness, stiffness and compressibility parameters have a strong influence on performance.

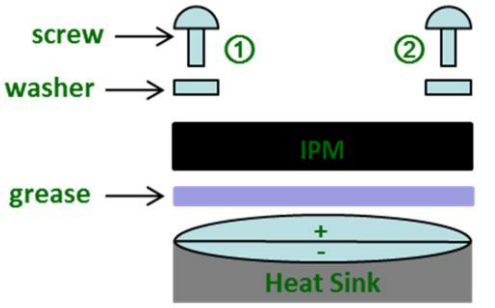


Figure 24. Mount IPM on a Heat Sink

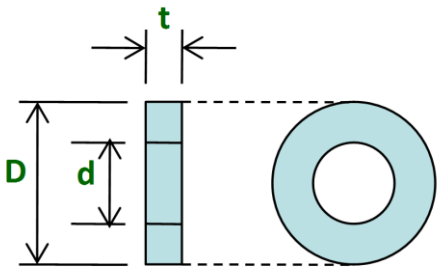


Figure 25. Size of Washer

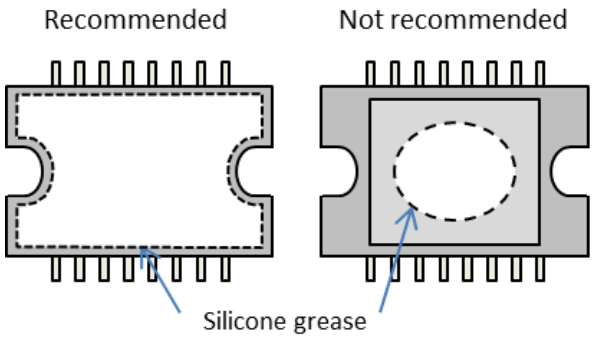


Figure 26. Uniform Application of Grease Recommended

Steps to mount an IPM on a heat sink:

1. Temporarily tighten maintaining a left/right balance.
2. Finally tighten maintaining a left/right balance.

Mounting and PCB Considerations

In designs in which the PCB and the heat sink are mounted to the chassis independently, use a mechanical design which avoids a gap between IPM and the heat sink, or which avoids stress to the lead frame of IPM by an assembly that slipping IPM is forcibly fixed to the heat sink with a screw.

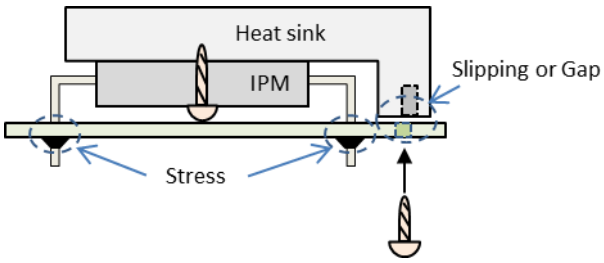


Figure 27. Fix to Heat Sink

Maintain a separation distance of at least 1.5 mm between the IPM case and the PCB. In particular, avoid mounting techniques in which the IPM substrate or case directly contacts the PCB.

Do not mount IPM with a tilted condition for PCB. This can result in stress being applied to the lead frame and IPM substrate could short out tracks on the PCB. If stress is given by compulsory correction of a lead frame after the mounting, a lead frame may drop out.

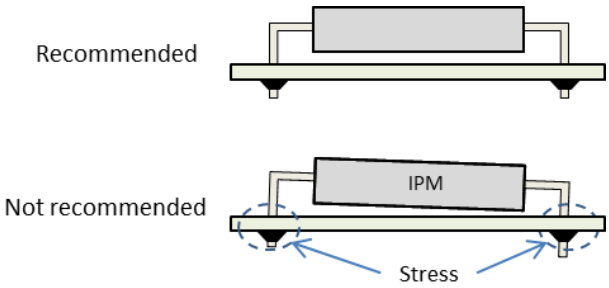


Figure 28. Mounting Position on PCB

Since the use of sockets to mount IPM can result in poor contact with IPM leads, we strongly recommend making direct connections to PCB.

Mounting on a PCB:

1. Align the lead frame with the holes in the PCB and do not use excessive force when inserting the pins into the PCB. To avoid bending the lead frames, do not try to force pins into the PCB unreasonably.
2. Do not insert IPM into PCB with an incorrect orientation, i.e. be sure to prevent reverse insertion. IPMs may be destroyed or suffer a reduction in their operating lifetime by this mistake.
3. Do not bend the lead frame.

Cleaning

IPM has a structure that is unable to withstand cleaning. Do not clean independent IPM or PCBs on which an IPM is mounted.

PACKAGE OUTLINE

The package of STK5C4U332J−E is DIP−S shown in Figure 29.

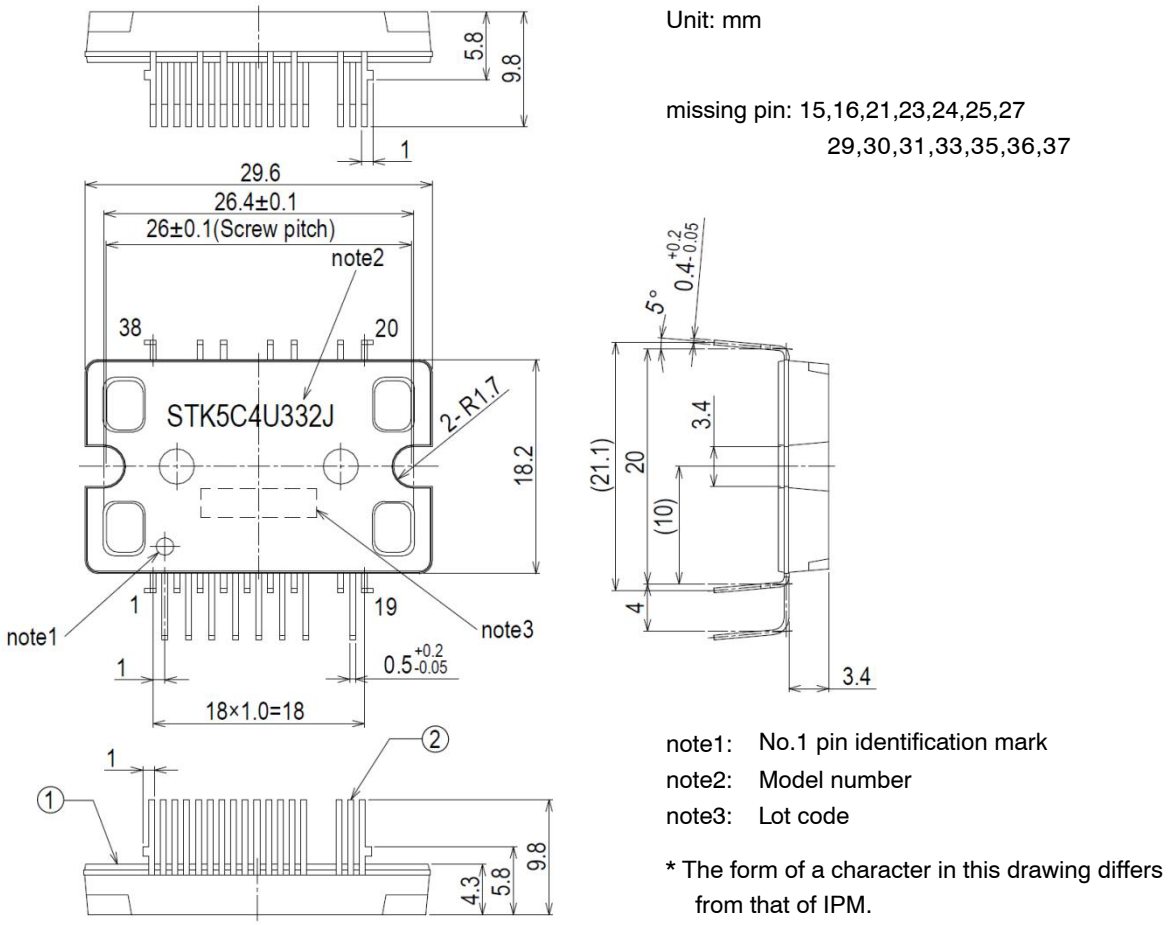
The package of NFAQxx60xx3x series is DIP−S6(Standard) shown in Figure 30.

The package of NFAQxx60xx6x series is DIP−S6(Short) shown in Figure 31.

The package of NFAQxx60xx3x series is DIP−S6(Standard with stopper) shown in Figure 32.

Package Outline and Dimension

STK5C4U332J−E (DIP−S)



Unit: mm

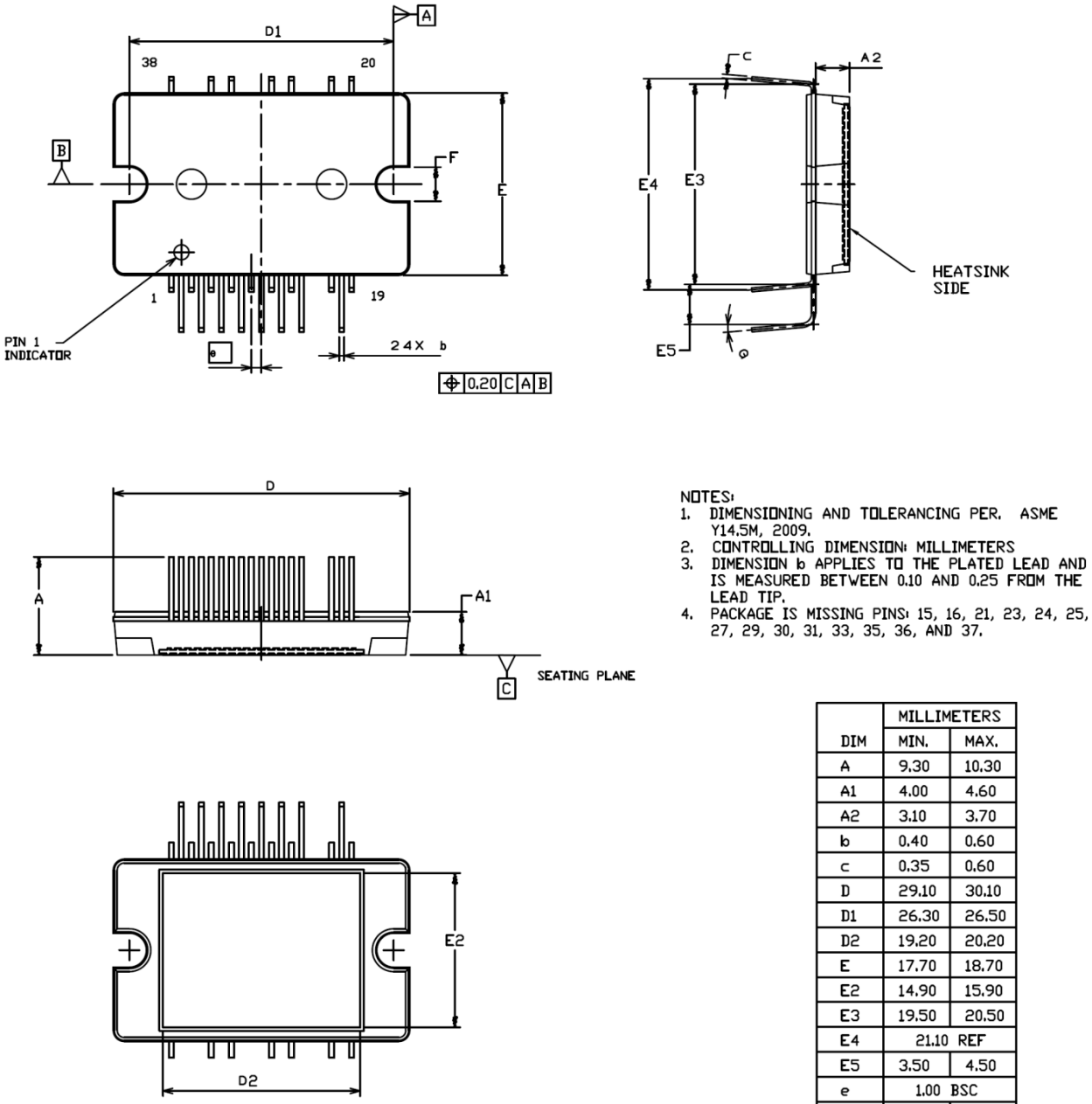
missing pin: 15,16,21,23,24,25,27
29,30,31,33,35,36,37

note1: No.1 pin identification mark
note2: Model number
note3: Lot code

* The form of a character in this drawing differs from that of IPM.

Figure 29. DIP−S Package Outline

NFAQxx60xx3x series (DIP−S6_Standard)

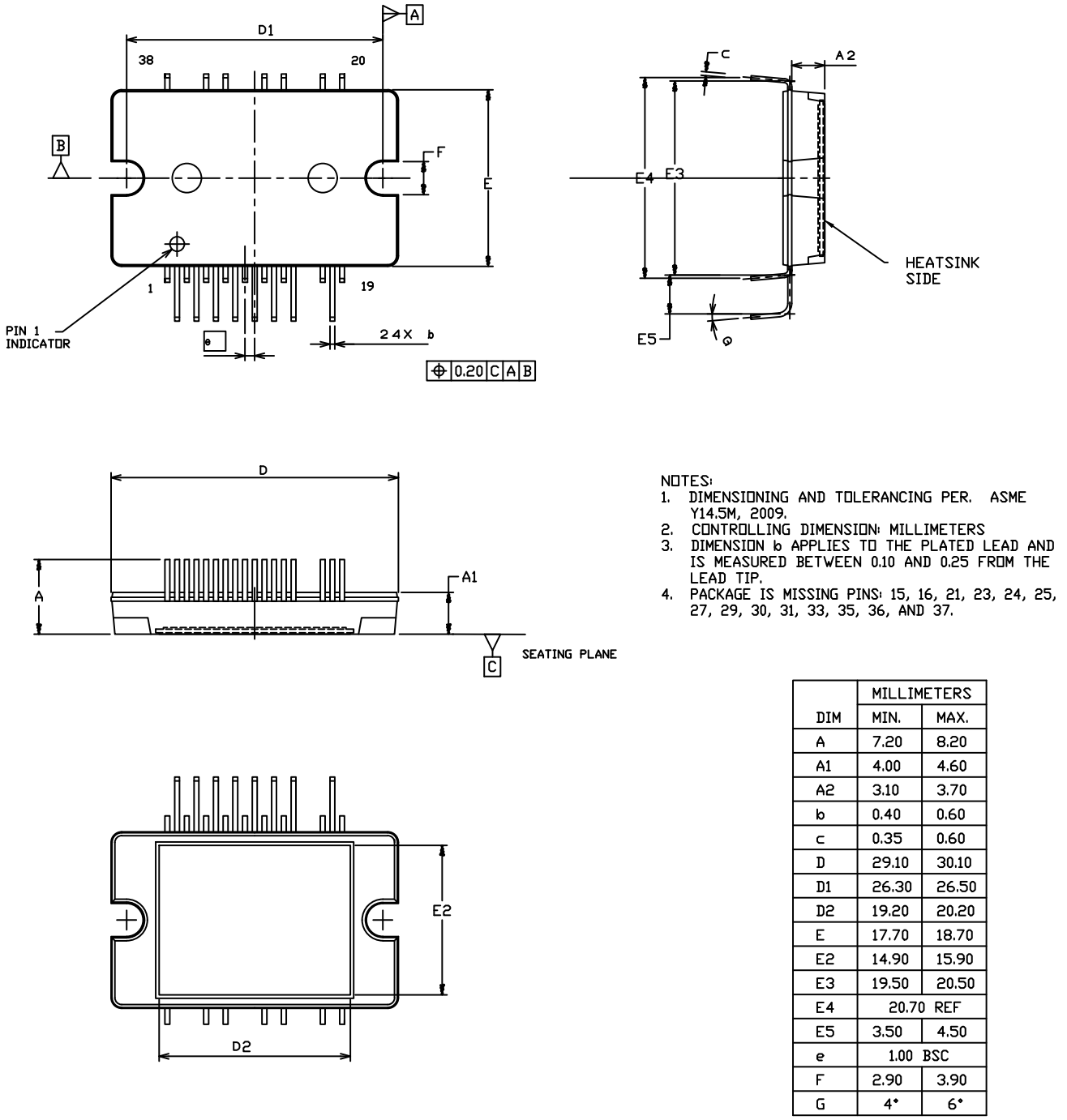


NOTES:
1. DIMENSIONING AND TOLERANCING PER. ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO THE PLATED LEAD AND IS MEASURED BETWEEN 0.10 AND 0.25 FROM THE LEAD TIP.
4. PACKAGE IS MISSING PINS: 15, 16, 21, 23, 24, 25, 27, 29, 30, 31, 33, 35, 36, AND 37.

	MILLIMETERS	
DIM	MIN.	MAX.
A	9.30	10.30
A1	4.00	4.60
A2	3.10	3.70
b	0.40	0.60
c	0.35	0.60
D	29.10	30.10
D1	26.30	26.50
D2	19.20	20.20
E	17.70	18.70
E2	14.90	15.90
E3	19.50	20.50
E4	21.10 REF	
E5	3.50	4.50
e	1.00 BSC	
F	2.90	3.90
G	4°	6°

Figure 30. DIP−S6 (Standard) Package Outline

NFAQxx60xx6x series (DIP−S6_Short)

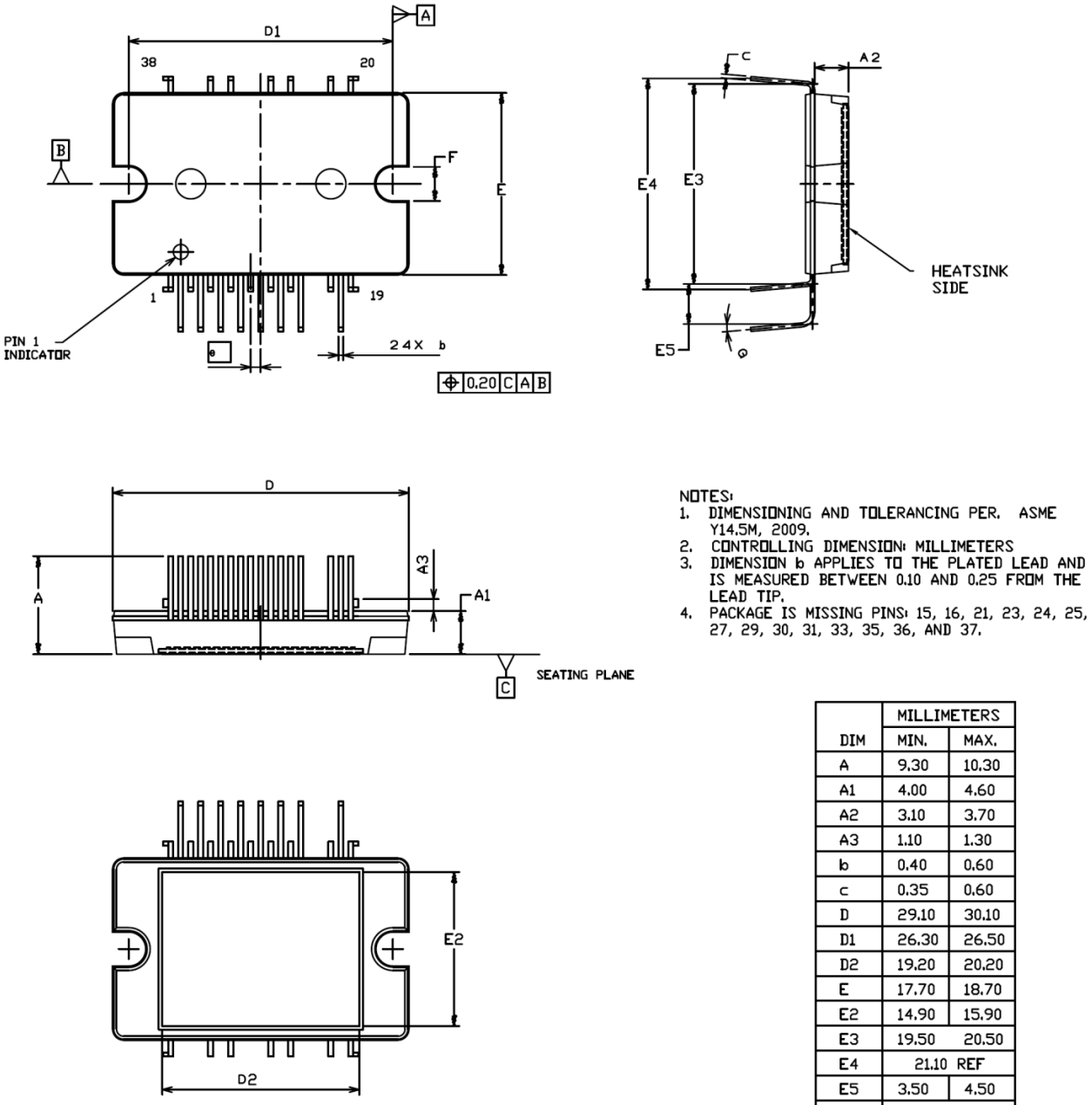


NOTES:
1. DIMENSIONING AND TOLERANCING PER. ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO THE PLATED LEAD AND IS MEASURED BETWEEN 0.10 AND 0.25 FROM THE LEAD TIP.
4. PACKAGE IS MISSING PINS: 15, 16, 21, 23, 24, 25, 27, 29, 30, 31, 33, 35, 36, AND 37.

	MILLIMETERS	
DIM	MIN.	MAX.
A	7.20	8.20
A1	4.00	4.60
A2	3.10	3.70
b	0.40	0.60
c	0.35	0.60
D	29.10	30.10
D1	26.30	26.50
D2	19.20	20.20
E	17.70	18.70
E2	14.90	15.90
E3	19.50	20.50
E4	20.70 REF	
E5	3.50	4.50
e	1.00 BSC	
F	2.90	3.90
G	4°	6°

Figure 31. DIP−S6 (Short) Package Outline

NFAQxx60xx3x series (DIP−S6_Standard with stopper)



NOTES:
1. DIMENSIONING AND TOLERANCING PER. ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO THE PLATED LEAD AND IS MEASURED BETWEEN 0.10 AND 0.25 FROM THE LEAD TIP.
4. PACKAGE IS MISSING PINS: 15, 16, 21, 23, 24, 25, 27, 29, 30, 31, 33, 35, 36, AND 37.

	MILLIMETERS	
DIM	MIN.	MAX.
A	9.30	10.30
A1	4.00	4.60
A2	3.10	3.70
A3	1.10	1.30
b	0.40	0.60
c	0.35	0.60
D	29.10	30.10
D1	26.30	26.50
D2	19.20	20.20
E	17.70	18.70
E2	14.90	15.90
E3	19.50	20.50
E4	21.10 REF	
E5	3.50	4.50
e	1.00 BSC	
F	2.90	3.90
G	4°	6°

Figure 32. DIP−S6(Standard with stopper) Package Outline

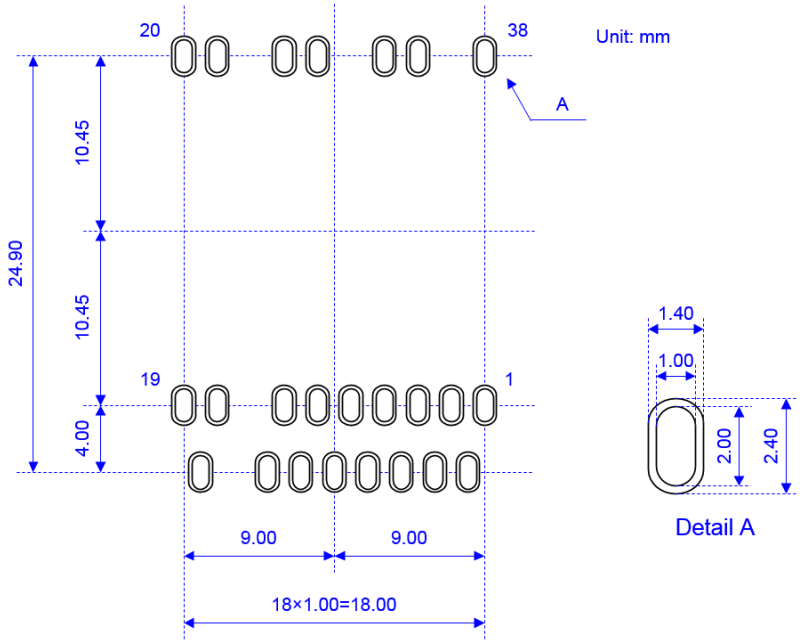


Figure 33. Recommended Land Pattern

Table 6. PIN OUT DESCRIPTION

Pin	Name	Description
1	VSS	Negative Main Power Supply
2	VDD	+15 V Main Power Supply
3	HINU	Logic Input for High−side Gate Driver − Phase U
4	HINV	Logic Input for High−side Gate Driver − Phase V
5	HINW	Logic Input for High−side Gate Driver − Phase W
6	LINU	Logic Input for Low−side Gate Driver − Phase U
7	LINV	Logic Input for Low−side Gate Driver − Phase V
8	LINW	Logic Input for Low−side Gate Driver − Phase W
9	FAULT	Fault Output
10	ITRIP	Shut Down Input
11	SD	Enable Input
12	CFOD	Fault Clear Time Setting
13	TH1	Thermistor
14	TH2	Thermistor
17	NU	Low−side Emitter Connection − Phase U
18	NV	Low−side Emitter Connection − Phase V
19	NW	Low−side Emitter Connection − Phase W
20	W	Phase W Output / High−side Floating Supply Offset Voltage
22	VBW	High−side Floating Supply Voltage − Phase W
26	V	Phase V Output / High−side Floating Supply Offset Voltage
28	VBV	High−side Floating Supply Voltage − Phase V
32	U	Phase U Output / High−side Floating Supply Offset Voltage
34	VBU	High−side Floating Supply Voltage − Phase U
38	P	Positive Bus Input Voltage

1. Pins 15, 16, 21, 23, 24, 25, 27, 29, 30, 31, 33, 35, 36, 37 are not present.

EVALUATION BOARD

The evaluation board consists of the minimum required components such as snubber capacitor and bootstrap circuit elements of the Compact IPM series.

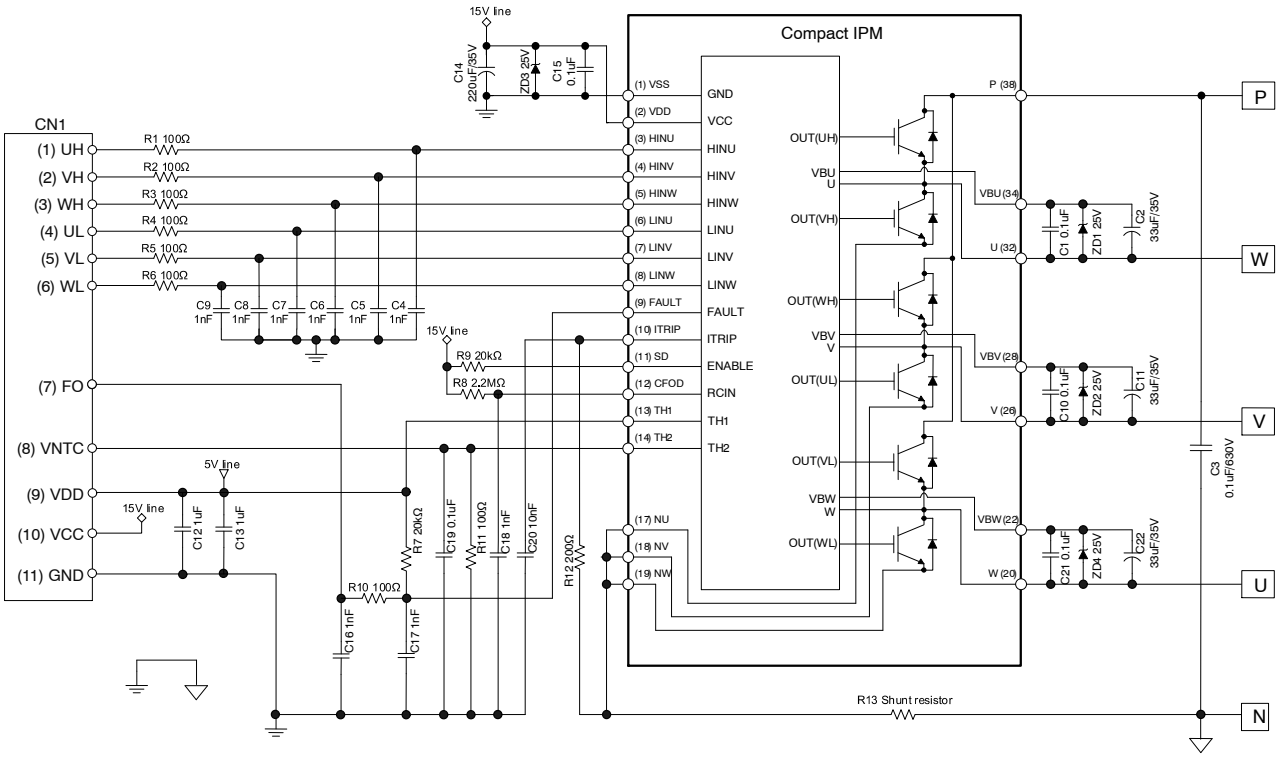
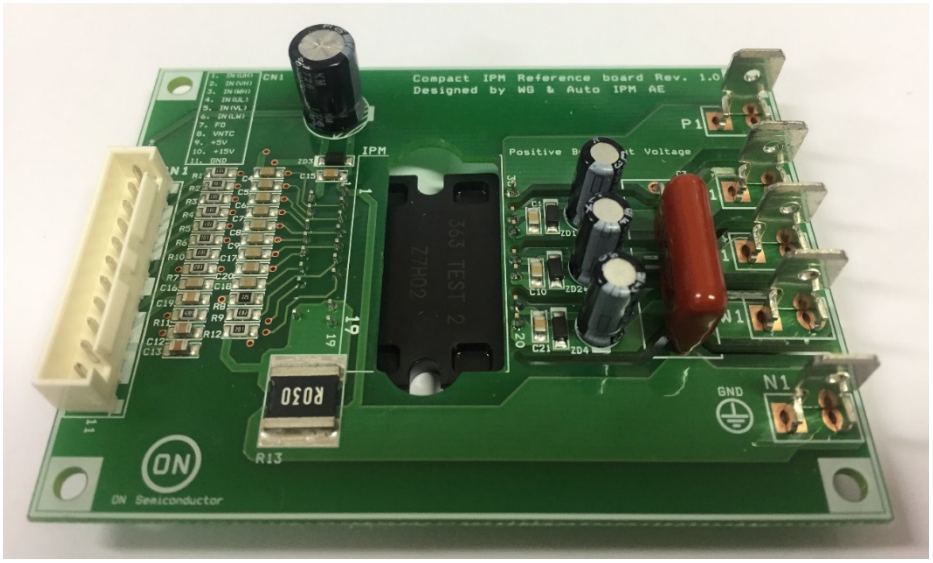


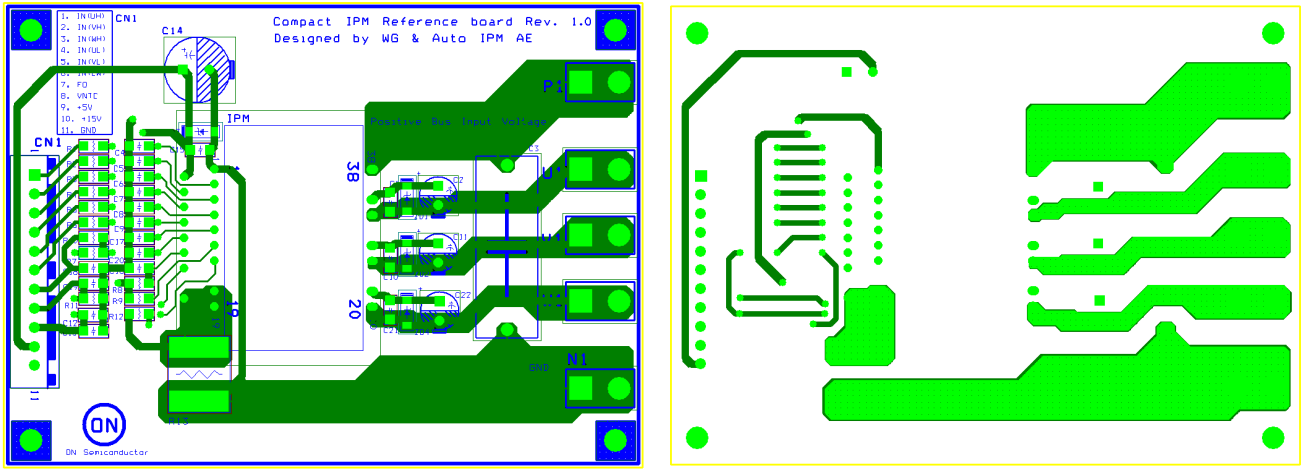
Figure 34. Evaluation Board Schematic



Length: 60 mm
Side: 83 mm
Thickness: 1.6 mm

Rigid double−sided substrate
Material: FR−4
Copper foil thickness: 35 um
Top side with resist coating.

Figure 35. Photo of Evaluation Board



Top side

Back side

Figure 36. PCB Layout (TOP View)

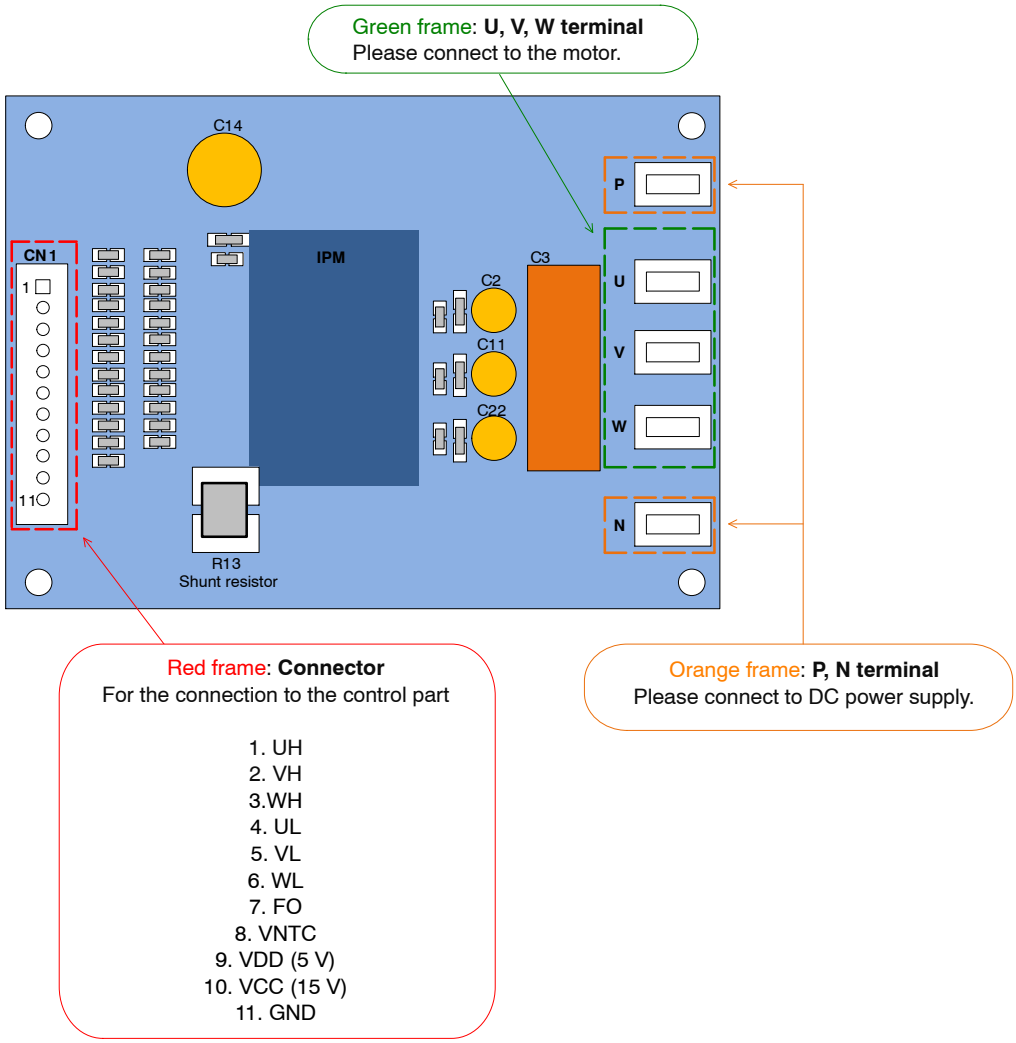


Figure 37. Description of Each Pin

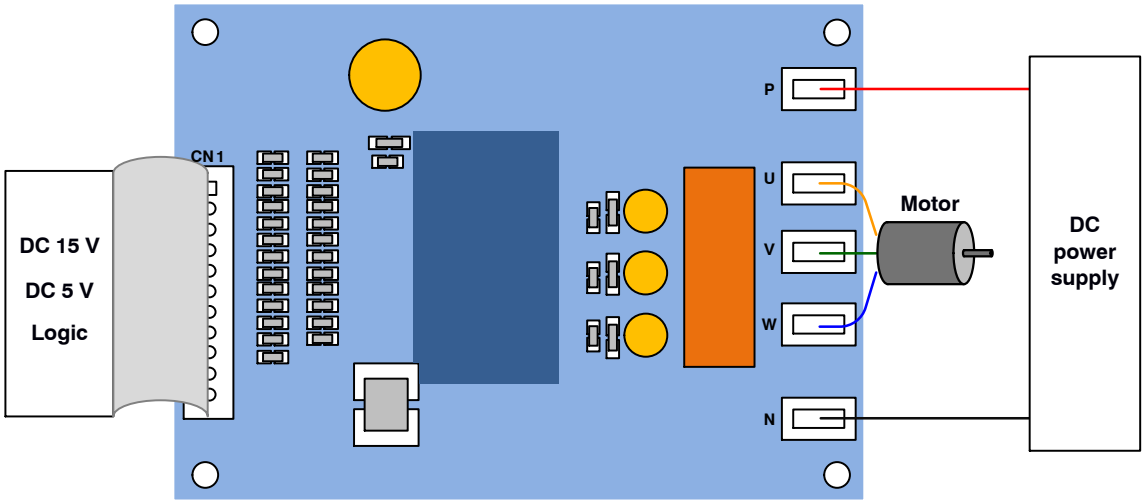


Figure 38. Connection Example

Operating Procedure

Step 1

Please connect each power supply, logic parts, and the motor to the evaluation board, and confirm that each power supply is OFF at this time.

Step 2

Please impress the power supply of DC 15 V.

Step 3

Please impress the power supply of DC 5 V.

Step 4

Please perform a voltage setup according to specifications, and impress the power supply between the “P” and the “N” terminal.

Step 5

By inputting signal to the logic part, IPM control is started. (Please set electric charge to the boot−strap capacitor of upper side by turn on lower side IGBT before running.)

NOTE: When turning off the power supply part and the logic part.
Please carry out in the reverse order to above steps.

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